Advanced Interface Bus (AIB) Die-to-Die PHY Deep Dive

**AIB Deep Dive Kickoff**: David C. Kehlet, Research Scientist, Intel

**AXI Protocols for Die-to-Die Interoperability**: Nij Dorairaj, Senior Engineer, Intel

**AIB and Chiplet Interface Generators**: Dr. Krishna Settaluri, President and Co-Founder, Blue Cheetah Analog Design, Inc.

**AIB-O: A Cost-Optimized Solution for the Chiplet Ecosystem**: Lai Guan Tang, Principal Engineer, Intel

**Die-to-Die Standards for 3D Heterogenous Integration**: Dr. Farhana Sheikh, Senior Engineer, Intel

**Innovating Intel FPGAs with the AIB Chiplet Ecosystem**: Martin Won, Senior Member of Technical Staff, Intel
Advanced Interface Bus (AIB) Die-to-Die PHY Deep Dive: AIB Deep Dive Kickoff

David C. Kehlet, Research Scientist, Intel
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AIB Deep Dive Kickoff

• AIB Origins
  › A solution to an FPGA die disaggregation challenge
  › Took advantage of the 7-8x wiring density increase of advanced packaging

• Enables high performance Heterogeneous Integration

• AIB called out as design parameter of US Government RAMP program

Image: Jariet Technologies, Inc.

Image: Jariet Technologies, Inc.

Rapid Assured Microelectronics Prototypes using Advanced Commercial Capabilities (RAMP) Phase 2

The Government is interested in selecting one Chiplet design that uses the packaging and interface technology developed in the State-of-the-Art Heterogeneous Integration Prototype (SHIP) program.

Chiplet:
1. > 5M gates w/o memory
2. Uses AIB (Advanced Interface Bus) and/or AIB-2 interface protocols for I/Os
3. Coordinated with the SHIP program for packaging and test
4. Must incorporate full production test capability, including DFT, ATPG, designer will provide test vectors, test coverage.

Source: NSTXL Consortium Prototype Project Request for Designs, Project No. 20-06
AIB Timeline

- Continuing the Commitment to Open Standards and Open Source!
- AIB 1.0 Open Source Hardware PHY: 2/2019
- AIB 1.0 CHIPS Alliance Released Specification: 12/2019
- AIB PHY Generator Open Source: 5/2020
- AIB 2.0 CHIPS Alliance Released Specification: 2/2021
- AIB 2.0 Open Source PHY Model: 2/2021
- AIB-3D Draft: This quarter!
AGENDA, AIB Deep Dive

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• **AIB and Chiplet Interface Generators**: Dr. Krishna Settaluri, President and Co-Founder, Blue Cheetah Analog Design, Inc.

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Advanced Interface Bus (AIB) Die-to-Die PHY Deep Dive: Protocols For Die-to-Die Interfaces

Nij Dorairaj, Sr. Engineer, Intel
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Outline

▪ How are modern designs built?
▪ Need for Standard Protocols
▪ AXI4 over AIB
▪ Channel Alignment
▪ Open Source
How are modern designs built?

- Designs are IP-based connected over **standard protocol interfaces** across MCPs, die and chips
- Example: FPGA based system
Need For Standard Protocols

- Customers are looking for die-to-die solution beyond PHY interoperability
- AXI4 is industry standard for ASIC interconnect
- Enabling chiplet to chiplet connectivity over AXI
  - Building AXI4 protocol adapter over chiplet to connect IP blocks
  - AXI IP for die-to-die eases the chiplet development time & expense
Foundational Die-to-Die Protocol: Streaming

- Streaming Protocol Requirements Summary
  - Parallel data width varies by application
  - Optional Valid indicator from source
  - Optional Ready indicator from destination
  - User frames their own data
  - High utilization/efficiency of the die-to-die PHY
  - Low latency
  
  ➔ *Looks like AXI4 Stream!*
Foundational Die-to-Die Protocol: Addressed Reads/Writes

- Memory application characteristics:
  - High utilization/efficiency of the die-to-die PHY
  - Low latency
  - Efficiently multiplexes my SoC's reads & writes
  - Memory clock asynchronous to the transfer clock
  - Looks like AXI4!

- Control and Status Registers application characteristics:
  - Moderate performance requirements
  - Economize on die-to-die utilization
  - Looks like AXI4-lite!
AXI4 over AIB enables end to end AXI4 connectivity between and within chiplets.
AXI4 over AIB

- Leader must react to the follower’s READY within the same cycle that READY is asserted.
- Straight AXI4 does not work for die-to-die:
  - Clock phase difference between leader and follower
  - Pipeline delays crossing between leader and follower
- Need adapters for AXI4 die-to-die operation, to allow for phase delays & pipeline delays
  - Adapters implement a credit scheme
  - The local Ready at the leader is HI when credits at the Leader-side adapter are available
  - Leader-side adapter decrements credit count on every Valid beat
  - Follower-side returns a credit when an entry is vacated in the follower-side adapter
  - Leader-side adapter increments the credit count when a credit return is received
AXI4 Stream Mapping Over AIB

<table>
<thead>
<tr>
<th>Leader to Follower 79b AXI4-Stream with TVALID on AIB</th>
<th>79</th>
<th>78</th>
<th>1</th>
<th>0</th>
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<tr>
<td></td>
<td>D[78:0]</td>
<td>Push</td>
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<table>
<thead>
<tr>
<th>Follower to Leader Credit Return on AIB 2.0Gen2 Full Rate</th>
<th>79</th>
<th>78</th>
<th>1</th>
<th>0</th>
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</thead>
<tbody>
<tr>
<td>Credit Reserved for AXI-Stream going Follower to Leader</td>
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<table>
<thead>
<tr>
<th>Leader to Follower 80b AXI4-Stream, No TVALID on AIB</th>
<th>79</th>
<th>78</th>
<th>1</th>
<th>0</th>
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<tr>
<td></td>
<td>D[79:0]</td>
<td></td>
<td></td>
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</tbody>
</table>

- We will allow non-byte quantities of TDATA for AXI4-Stream to maximize channel bandwidth utilization

AXI4 Adapter maps AXI to AIB
Mapping shown at this point
- All 5 channels of AXI are sent across AIB wires
- Example: write transaction starts with address on AW channel followed by a write data on W channel and a response on B channel
**AXI4 Mapping Over AIB**

- **Simple example:** 64b data bus over a AIB2.0Gen2 channel at full rate
  - `awpush` and `wpush` are "valid" indicators and use up credits in the adapter
  - Write response comes back the other way with credit bits
Open Source

- AXI4, Channel Alignment IP and IP Generator will be released as open source code with permissive Apache-2.0 license
  - Repository established: [https://github.com/chipsalliance/aib-protocols](https://github.com/chipsalliance/aib-protocols)
- Release: End 2021
- Support for 3 years
Data Skew Across AIB

- Protocols transfer data over multiple channels
- Data across AIB is skewed due to:
  - Clock insertion delay on channels
  - EMIB wire trace differences
  - Physical variation
- For correct operation data needs to come out aligned
AXI4 and Channel Alignment

- AXI adapters automatically instantiate channel alignment IP for achieving alignment for AXI protocol.

- How this is done:
  - One of the data bit is used as strobe bit on all channels.
  - It is set to be asserted periodically.
  - Channel alignment block deskews the data using the strobe signal.
  - After the initial training phase once the alignment is achieved the strobe bits can be used for application data.
AIB and Chiplet Interface Generators

Krishna T. Settaluri, President and Cofounder, Blue Cheetah
Blue Cheetah Overview

Rapidly configurable, software-driven, leading edge, process portable
Blue Cheetah’s Origin Story

• Based on pioneering research from UC Berkeley, began in 2010

• Key technical differentiator – “designer in the driver seat” not ”replace the designer & automate analog…”

• Powerful API to allow creation of design procedures and process-portable interface to layout

J. Crossley et al., ICCAD 2013
E. Chang et al., CICC 2018
Our Approach: **Generator-Based Design**

- **Draw/(Re-)Size Schematic (Virtuoso)**
- **Verify specs (simulate)**
- **(Re-) Draw Layout (Virtuoso)**

Capture designer knowledge in executable generator

Re-use design methodology

Enable parameterization and process migration

Our approach is *not*
- Optimization engine
- Place-and-router
- GDS porter

Final outputs

- **netlist**
- **GDS**
- **LEF**
- **LIB**
- **Bmod**
- **Soft IP (RTL + constraints)**

Generator framework enables industry-standard design collateral
## Silicon Proven Highlights

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<th>2021</th>
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<td>Q2</td>
<td>Q3</td>
<td>Q4</td>
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<td>Die-to-Die Interfaces</td>
<td>Die-to-Die Interfaces</td>
<td>Die-to-Die Interfaces</td>
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<td>AIB1.0, 2ch</td>
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<td></td>
<td>Intel22FFL tapeout*</td>
<td>A/MS circuit generators open sourced</td>
<td>Silicon validated at 2Gbps*</td>
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<td>Silicon test</td>
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<td>Tapeout</td>
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<td>Q3</td>
<td>Q4</td>
<td>Q1</td>
<td>Q2</td>
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<td>Memory Interfaces</td>
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<td></td>
<td>LPDDR4x PHY*</td>
<td>Custom In-Package DRAM PHY*</td>
<td>Silicon test</td>
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<td></td>
<td>Silicon test</td>
<td>Silicon test</td>
<td>Silicon test</td>
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</table>

- Generators are backbone of success & enabled rapid design with aggressive performance
- Designed on advanced finFET nodes, with AIB generators open sourced to drive awareness

*disclosed with permission
AIB1.0 Highlights

• Developed **full generators** for all custom circuits (e.g. driver, phase interp., etc.)
  • Intel 22FFL silicon demonstrated communication at 2Gbps with Intel Stratix-10 FPGA
  • Press release

(disclosed with permission)
Memory Interface Highlights

- Fully featured memory PHYs with industry standard interfaces

**LP4X PHY:**
Dual-Rank 1x16 @ 4266MT/s, <1.5pJ/bit

**Custom in package DRAM PHY:**
Dual-channel 1x68 @ 2133MT/s, <750fJ/bit

- Generators enabled automated PHY circuit block generation and parameterized assembly

- Multiple PHYs integrated into a 14/16nm finFET SoC
What’s Next: Generators & Interfaces – A Natural Fit

- The **chiplet interface** market is gaining tremendous momentum through adoption by the USG, tier 1 semiconductor companies, and emerging AI / ML edge startups

- But, chiplet interface standards are the Wild Wild West!
  - No single chiplet interface standard has ‘won’ (likely multiple winners) eg. AIB, BoW, OpenHBI, …
  - Early projections of $100m+ revenue YOY

- Chiplet ecosystem crucially needs value of generators
  - **Configurability and ease of use** – configurable standard, packaging, data rate, …
  - **State-of-the-art PPA** – no compromise to performance
  - **Faster time to market** – iterate at software speeds
  - **Reduced risk** – ‘compiler’ based approach ensures predictable design results

![SoC SAM by Market Segment](image_url)
Blue Cheetah Company Overview

• Founded in May 2018

• Led by globally-recognized experts in A/MS IP and design methodologies

• Global team with 25+ employees and growing fast!

• Full stack expertise – analog, digital, software, PDK, firmware

• For more info, visit www.bluecheetah.com or email info@bcanalogue.com
AIB-O: A Cost-Optimized Solution for the Chiplet Ecosystem

Lai Guan Tang, Principal Engineer, Intel
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Outline

- Die Disaggregation Technology Background
- AIB-O: Cost-optimized D2D interconnect for chiplets
- AIB-O Bump Plan Consideration
Die Disaggregation Technology Overview

**Low Density: 2D Disaggregation**

- **D2D with on-pkg traces**
- **Low wire density**

**Pros:** Lowest Cost

**Cons:** Limited D2D BW@ISO Power

**Med Density: 2.5D Disaggregation**

- **D2D through advance package,** i.e. EMIB, si-interposer, RDL
- **Medium wire density**

**Pros:** Higher BW @ISO Power

**Cons:** Medium Cost

**High Density: 3D Disaggregation**

- **D2D through base die**
- **High wire density**

**Pros:** Form Factor advantage

**Cons:** Highest Cost
Generation of AIB Interfaces

- Multiple generations of AIB over different packaging technologies.
- Optimize for different bandwidth, price point and power.
- Preserving interoperability for multiple generations to enable chiplet reuse.
Common AIB PHY Concept: AIB2.0 or AIB-O

- Single physical design at the AIB channel level to scale for different bandwidth density
  - AIB 2.0 or AIB-O
  - Connect different number of IO in C4 vs ubumps
  - RDL layer change to re-bump ubump to C4
- Enable disaggregation benefit without high packaging cost
- 2 Layers + 1 micro- stripline for D2D routing. Can be enabled on 5-2-5 package.
AIB-O Bump Plan

- TX bump field at die edge
- To maximize signals density, maintain 312.48um per channel shoreline and meeting performance, near-end and far-end bump field are not rotatable.
- For a chiplet to pair with itself for debug, testing purpose, some data swizzling at PHY will be required.
- Clocks are rotatable.
Package Routing

1st layer
Micro-stripline

2nd layer
Stripline

3rd layer
Stripline

8 signals per layer. 3 layers for 24 AIB-O signals
Summary

- AIB-O provides a cost-optimized D2D interconnect for chiplets.
- Single PHY to scale for different BW density.
- Maximize BW density with commonly used package layer form factor.
Advanced Interface Bus (AIB) Die-to-Die PHY Deep Dive:
Die-to-Die Standards for 3D Heterogeneous Integration

Dr. Farhana Sheikh, Senior Engineer, Intel

David C. Kehlet, Research Scientist, Intel
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Motivation: 3D ICs and 2.5D D2D PHY Interfaces

• Increasing use of 3D integration outside of just stacked memories
  › Example: Intel Lakefield (logic-on-logic) [W. Gomes, ISSCC 2020]

• 3D ICs: stacked silicon wafers or dies that are interconnected using through-silicon vias (TSVs) or Cu-Cu connections

• 3D ICs typically designed together by same set of designers or same company
  › Proprietary or simple interfaces, e.g., SRAM memory interface in the vertical direction

• Chiplet ecosystem in vertical direction requires standard interfaces
  › Incorporate into designs to enable 3rd party chiplet integration vertically

• AIB 1.0 and AIB 2.0 are opensource D2D PHY interfaces that enable high-performance interconnect → basis for 3D opensource standard
## Some 2.5D D2D PHY Standards

<table>
<thead>
<tr>
<th>Serial Link</th>
<th>Signaling</th>
<th>Technology</th>
<th>Channel</th>
<th>Reach (mm)</th>
<th>Data Rate (Gbps) Per Wire</th>
<th>Energy (fJ/b)</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ground referenced signaling</td>
<td>SE</td>
<td>28nm</td>
<td>On-chip</td>
<td>1.5</td>
<td>16</td>
<td>255</td>
<td>1-hop used as proxy for interposer</td>
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<tr>
<td>Voltage-Mode Tx with Passive EQ</td>
<td>SE</td>
<td>28nm</td>
<td>Interposer</td>
<td>2.5</td>
<td>20</td>
<td>300</td>
<td>Does not include clocking power</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.5</td>
<td>18</td>
<td>320</td>
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<tr>
<td>TSMC LIPINCON</td>
<td>SE</td>
<td>16nm</td>
<td>InFO</td>
<td>0.55</td>
<td>2.8</td>
<td>424</td>
<td>0.3V I/O voltage</td>
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<tr>
<td></td>
<td>SE</td>
<td>7nm</td>
<td>Interposer</td>
<td>0.5</td>
<td>8</td>
<td>560</td>
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<tr>
<td>Intel AIB 2.0</td>
<td>SE</td>
<td>-</td>
<td>Interposer, MCM</td>
<td>10</td>
<td>4.0 - 6.4</td>
<td>500</td>
<td>0.4V I/O voltage, 45um / 55um EMIB support</td>
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<tr>
<td>Bunch of Wires (BoW)</td>
<td>SE</td>
<td>14nm</td>
<td>MCM / Interposer</td>
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<td>5</td>
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<td>MCM</td>
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<tr>
<td>MediaTek MLINK</td>
<td>SE</td>
<td>7nm</td>
<td>InFO, CoWoS</td>
<td>&lt;1</td>
<td>12.8 (InFO), 20 (CoWoS)</td>
<td>460 - 500</td>
<td>48um pitch InFO, 40um pitch CoWoS</td>
</tr>
</tbody>
</table>

References: Forum 5, ISSCC 2021; VLSI 2021

- Generator-based analog/mixed-signal + behavioral RTL
- Flexible across process
- Agnostic across D2D integration fabric (e.g., EMIB, interposer, …)
- Opensource

AIB-3D based on AIB2.0

Desire similar features as 2D interface
3D PHY Standards: Existing and Requirements

Existing 3D PHY interfaces:
• HBM2, HBM2E, HBM3, Glink-3D [1]
  › Memory-centric or early stages and not open-sourced

Requirements:
• Scalable across wide range of micro-bump and TSV pitch: future proof
• Single data rate
• Half-duplex or full-duplex operation - programmable
• Point-to-point or point-to-multipoint
• Can be used for Logic-on-Logic or Logic-on-Memory
• Integrated PLL/DLL
• Scalable number of channels
• Lane repair
• Built-in test and pattern checker
• Synthesizable or generator based soft-macro
• Non-intrusive power delivery

Reference: E. Beyne, imec, Forum 5.8, ISSCC 2021
Reference: AIB-3D Concept, F. Sheikh, Intel Corporation
Reference: J. Bausch, May 24, 2021, EE Times
AIB-3D High-Level Architecture

- Wider data bus configured with respect to bump pitch or TSV pitch
  
  - Examples:
    - 25µm bump pitch \(\leftrightarrow\) 512-bits TX or RX (half-duplex); 256-bit TRX (full-duplex) [32x32 array, 0.8 x 0.8 mm\(^2\)]
    - 10µm bump pitch \(\leftrightarrow\) 1024-bits TX or RX (half-duplex); 512-bit TRX (full-duplex) [46x46 array, 0.46 x 0.46 mm\(^2\)]

- AIB-3D “patch”:
  
  - 2Gbps per bump (based on native logic speed)
  - Max. Bandwidth / mm\(^2\): 1600 [25µm bump pitch]
  - Max. Bandwidth / mm\(^2\): 10,000 [10µm bump pitch]
  - Target: 1 to 2 cycle latency per direction
  - Include redundant bumps for repair
  - Integrated test and pattern generation
  - Self-protected I/Os via ESD: 3D drivers are smaller
  - Support for Logic-on-Logic or Logic-on-Memory
  - Initially point-to-point
    - Extension to point-to-multipoint in future
  - 32 x 32 array size (1024 x 25µm bumps)
    (512-bit channel + redundancy + power + control)
  - Array scales with 3D micro-bump / TSV pitch
  - Options:
    - Orientation, modular tiling, modes, configurable channels
AIB-3D Clocking

- Leverage AIB2.0 Base for lighter weight implementations that require minimal circuitry
- Single data rate (SDR) signaling where new data is transferred on one edge of the clock
- Input and output signals are registered (additional latency)
- Array has a single clock that is forwarded with TX data
- On return path, there is no forwarded clock (captured with controller die clock)
AIB-3D: Non-Intrusive Power Delivery

• Power delivery and thermal management is a challenge in 3D ICs
• Instead of forcing chiplets to incorporate power delivery to top die through the base chiplet (i.e., requires top die and base die co-design) leverage Foveros Omni [2] and Foveros Direct [3] to deliver power without compromising integrity of base die.
AIB-3D: Summary

- Increasing use of 3D integration outside of just stacked memories
- Chiplet ecosystem in vertical direction requires standard interfaces
- AIB 1.0 and AIB 2.0 are opensource D2D PHY interfaces that enable high-performance interconnect → basis for 3D opensource standard
- AIB-3D:
  - Over-die and shoreline support
  - Scalable to support μ-bump / TSV scaling
  - Process agnostic, opensource
  - Support logic-on-logic and logic-on-memory
  - Options: orientation, modular tiling of “AIB-3D patch”, configurable channels
  - Early specification in progress
Advanced Interface Bus (AIB) Die-to-Die PHY Deep Dive: Innovating Intel® FPGAs with the AIB Chiplet Ecosystem

Martin S. Won, Senior Member of Technical Staff, Intel
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Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

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This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

Intel estimated results are based on product specifications.
Rapid Silicon Innovation
Any Compute, Any Connect, Any Developer

Supported by Intel® eASIC™ device and ASIC power reduction paths

Chiplet Library

Process
- FPGA Core
- FPGA Core Optimized
- CPU
- Core with HPS

Move
- CXL
- UPI

Store
- Memory
- Memory
- Custom

Specialized
- RF
- Compute
- AI
- I/O
- Optical

Intel® Stratix® 10 Series
GX | SX | TX | MX | DX | NX

Intel® Agilex™ Series
F-Series | I-Series | M-Series

45%¹ performance improvement
Up to 40%¹ lower power
PCI Express Gen5
Compute Express Link (CXL)
116 Gbps Transceiver
Next Gen HBM2e

¹ - This Comparison is based on Intel® Agilex™ FPGA and SoC family vs. Intel® Stratix® 10 FPGA. Performance varies by use, configuration and other factors. Learn more at www.Intel.com/PerformanceIndex
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs

**INTEL CHIPLET LIBRARY**

- Compute
  - CPU
  - Structured ASIC
  - 14nm FPGA Fabric
- 14nm FPGA Fabric
- 14nm FPGA Fabric w/ Enhanced IP
- 10nm SuperFin FPGA Fabric

**Interconnect**

- CXL
- UPI
- Serial XCVR 28G
- PCIe Gen3
- PCIe Gen4
- PCIe Gen5
- Serial XCVR 58G
- Serial XCVR 116G

**Specialized**

- Network
- Accel.
- DSP
- Memory

**OTHER CHIPLETS**

- Custom Accel.
- Custom Compute
- AI
- Custom I/O
- Analog ADC/DAC
- Custom Protocol

Advanced Interconnect Bus

Open-source die-to-die interconnect standard
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs

INTEL CHIPLET LIBRARY

- **Compute**
  - CPU
  - Structured ASIC
  - 14nm FPGA Fabric
  - 14nm FPGA Fabric AI Enhanced
  - 10nm SuperFin FPGA Fabric

- **Interconnect**
  - CXL
  - UPI
  - Serial XCVR 28G
  - PCIe Gen3
  - PCIe Gen4
  - PCIe Gen5
  - PCIe Gen6
  - Serial XCVR 116G
  - Serial XCVR 58G

- **Specialized**
  - Network
  - Accel
  - DSP
  - Memory

OTHER CHIPLETS

- **Advanced Interconnect Bus**
  - Open-source die-to-die interconnect standard

- **Custom Accel**
  - Analog ADC/DAC
  - Custom Protocol
  - Custom Compute

High-Performance General-Purpose FPGA

Intel® Stratix 10 GX Architecture
Heterogeneous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs
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**OTHER CHIPLETS**

- Custom Accel.
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- Custom I/O
- Analog ADC/DAC
- Custom Protocol

* Optional

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*Open-source die-to-die interconnect standard*
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs
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Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs
# Growing AIB-Based Chiplet Portfolio

<table>
<thead>
<tr>
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### Technology & Foundry Agnostic

- **2 FPGA families**
- **6 XCVR/SERDES chiplets**
- **3 Optical chiplets**
- **3 Data converter chiplets**
- **2 ASIC compute chiplets**
- **5 Defense Industrial Base (DIB) partners and chiplets**
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**Technology & Foundry Agnostic**

- 2 FPGA families
- 6 XCVR/SERDES chiplets
- 3 Optical chiplets
- 3 Data converter chiplets
- 5 Defense Industrial Base (DIB) partners and chiplets
FPGA Optical Integration – Technology Pathfinding

- Ayar Labs optical chiplet enables pathfinding to FPGAs with integrated optical I/O
- Presented at Hot Chips 2019 (link)
- Demonstrated 2 Tbps in Q1 2020 (link)
- Announced prototype for 8 Tbps demo at OFC 2021 (link)

Assembled Prototype

- 5 optical chiplets => 5 x 1.6 Tbps: 8 Tbps
- Intel® 14nm FPGA fabric chiplet
- 1 electrical TRX chiplet (H-tile)

Goals: Increase Bandwidth, Reduce Latency, Lower Power

This research was, in part, funded by the DARPA PIPES (Photonics in the Package for Extreme Scalability) program HR0011-19-3-0003
Industry's Highest Sample Rate ADC/DAC Technology for FPGAs

System-in-Package heterogeneous FPGA with industry’s highest sample rate Direct RF data converter technology

Performance Leadership
5X higher bandwidth\(^1\)
Up to 64 Gsps sample rates\(^2\)
Latency, size, and power reduction

Extensible
Chiplet-based integration enhances Intel® custom logic continuum to enable more targeted FPGAs, SoCs, and ASICs

Target Applications
Radar and Electronic Defense
Test and Measurement
Wireless Comms

January 2021 Technology Announcement

\(^1\)Compared to Xilinx Zynq Ultrascale+ RFSoC Gen 3
\(^2\)Based on internal current estimates

For more complete information about performance and benchmark results, visit [www.intel.com/benchmarks](http://www.intel.com/benchmarks)
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs

INTEL CHIPLET LIBRARY

Compute
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- 14nm FPGA Fabric AI Enhanced
- 10nm SuperFin FPGA Fabric

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- UPI
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- Serial XCVR 58G
- PCIe Gen5
- PCIe Gen4
- PCIe Gen5
- Serial XCVR 116G

Specialized
- Network
- Accel.
- DSP
- Memory

Advanced Interconnect Bus
Open-source die-to-die interconnect standard

OTHER CHIPLETS

Custom Accel.
Custom Compute
AI

Custom I/O
Custom Protocol
Analog ADC/DAC

FPGA
eASIC™
ASIC

Analog Chiplet Integration Enables a More Capable Custom Logic Continuum
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs

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**OTHER CHIPLETS**

- Custom Accel.
- Custom Compute
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**Advanced Interconnect Bus**

Open-source die-to-die interconnect standard

**High-Performance, IO-Intensive Flexible Compute Product with Analog**

Potential FPGA Integrating ADC/DAC, PCIe Gen4 & 58G XCVRs
Heterogenous Integration of Interoperable Chiplets Builds More Targeted FPGAs & SoCs

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**OTHER CHIPLETS**

- **Advanced Interconnect Bus**
  - Open-source die-to-die interconnect standard

- **Power-Optimized, Custom Acceleration**
  - Structured ASIC with Analog

- **Potential eASIC Integrating**
  - ADC/DAC, PCIe Gen5, & Custom Acceleration Engine
Conclusion

▪ AIB-based chiplet design provides semiconductor product developers with several advantages:
  • Options to integrate functions regardless of process node / foundry / developer
  • Access to wider range of functions developed by chiplet ecosystem
  • Rapid product innovation

▪ AIB chiplet ecosystem enabling Intel® to pathfind new FPGA technology areas like optical and ADC/DAC integration
  • Integrating industry-leading ADC/DAC capabilities into future Intel FPGAs