Value and Opportunities in Open-Source for Circuit Design



Christoph Sandner, Senior Principal Infineon Technologies Austria AG <u>Christoph.sandner@Infineon.com</u>

Linux Foundation Open Source Summit Europe: Open Hardware Mini Summit, Vienna September 19, 2024







- Motivation for OS Hardware
- □ Relevant pillars:
 - 1. Education
 - 2. OS PDKs
 - 3. OS IP
 - 4. Disruptive Methods: (Analog Design) Automation
- To get Industry involved, OS has to provide value!!!

Why Hardware Collaboration?

s Create Culture

Emulate software success in hardware

Value is interdependent on competitors

Self-Interest

Innovation requires diverse ideas

Game Theory: Stag Hunt – Work together towards mutual benefit, rather than solving small problems on our own.

[S. Cetola, Intel]

Linux Foundation Open Source Summit Europe: O

The Problem

Workforce / Education:

- Lack of skilled EE resources
- Computer Science (CS) is more attractive
- <u>ittps://www.eetimes.com/chip-experts-see-talent-shortage-as-main-</u> EE is a complex topic to learn, no abstraction
- Barrier to get hands-on experience (do a chip tapeout) is very high

DESIGNLINES | SOC DESIGNLINE

By Alan Patterson 07.21.2023 🎵 3

Share Post f Share on Facebook Share on Twitter in

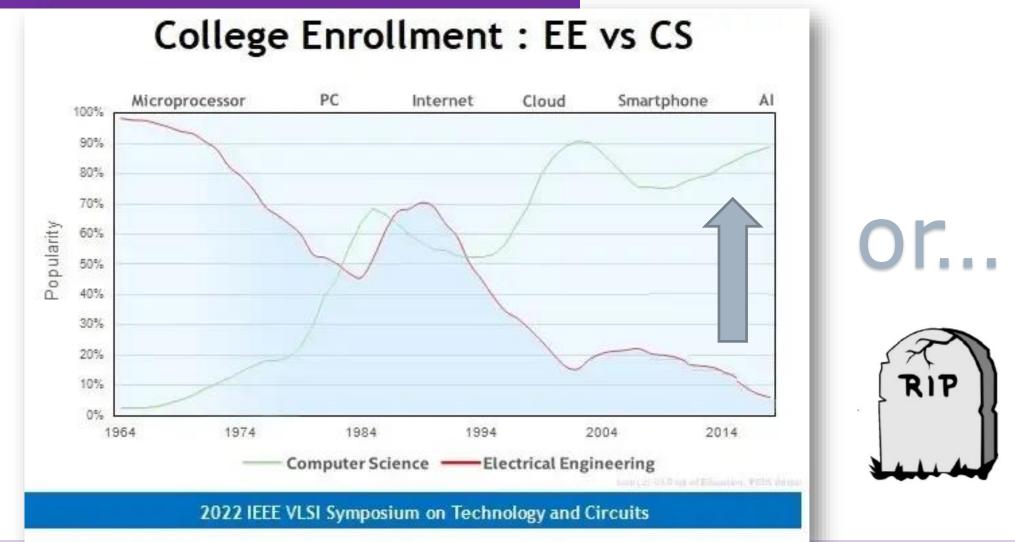
Chip Experts See Talent Shortage as Main Growth

□ R&D Efficiency, Time-To-Market:

- Industry competes on maximizing EBIT
- Complexity and effort of chip development increases by 2...4x for every node
- Analog IC design: Still many manual steps, lack of automation

Semiconductor Industry will die out...









Academia and Industry need to join forces! Open-Source to the rescue?



OS Success Story:

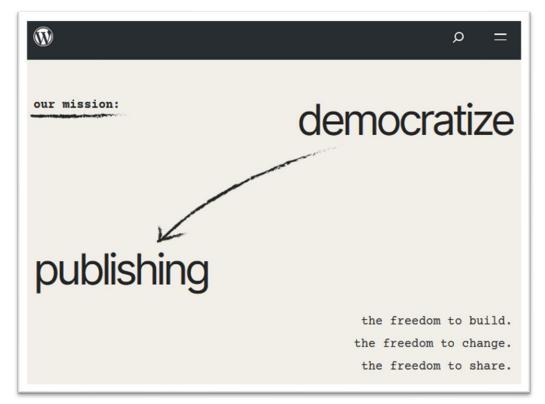


□ Free and OS Instruction Set Architecture (ISA)



OS Success Story: Wordpress

- WordPress powers 43% of websites
- Endless variety of plugins
 - \rightarrow Huge ecosystem
- □ Low entry hurdle
- Everyone can design and maintain a small website



□ Why not... "Democratizing IC Design"? © Boris Murmann



OS to the Rescue? - Education



https://sscs.ieee.org/about/solid-state-circuits-directions/ss

Home / About / Solid-State Circuits Directions / SSCS PICO Program SSCS PICO Program Democratizing IC Design: The SSCS PICO Program chips committed to improvindesigned through a integrated clicuity in we big browser by anyone, anywhere and through the construction ...help to accelerate the construction of the required ecosystem Outreach (PICO) program, the SSCS is working with the rapidly grow the construction of the required ecosystem. Our goal is to help build and connect to new communities that share our excitement about IC innovation and its democratization toward a new wave of global impact.



https://bit.ly/esscxxrc22-goog

□ Google, ESSICR2022:

Don't need to wait for your masters course to start with IC design...

Do your first tapeout in school!

r	1		1
Tape out	Student Level	Budget (USD)	Process Node
First	Middle School	<\$20	180nm / 130nm
Second	High School	\$20 → \$1,000	180nm → 90nm
Multiple	Undergrad	\$100 → \$10,000	90 nm \rightarrow 45nm
Advanced	Masters	>\$10,000	90nm → 22nm
Leading Edge	PhD	>\$50,000	<28nm 7nm / 5nm / 3nm

Future pathway for ASIC designer



OS to the Rescue? – PDKs

- □ 2020: SkyWater 130nm CMOS
 - https://github.com/google/skywater-pdk
- □ 2022: GlobalFoundries 180nm MCU
 - https://github.com/google/gf180mcu-pdk
- □ 2023: IHP 130nm BiCMOS
 - <u>https://github.com/IHP-GmbH/IHP-Open-PDK</u>
- **2**024: ?

Permissive Apache 2.0 licensing



OS to the Rescue? – Design System



- □ Growing number of OS design systems, eg:
 - OpenRoad, OpenFASOC, Chipyard, BAG, Align, Magic, OpenRAM, ...

Stefan Schippers sample.sch

□ Growing ecosystem:

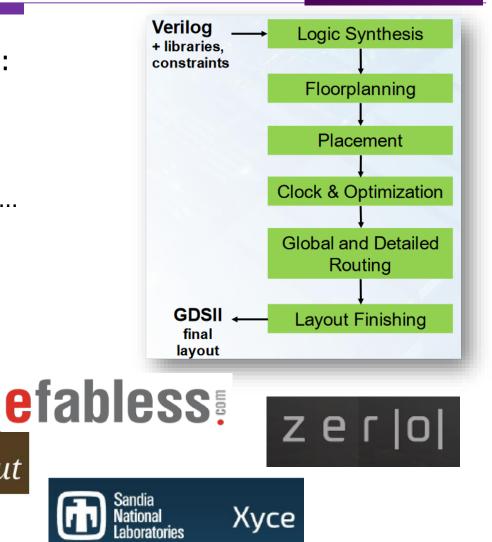
SCHEM

Current distribution version 8.2

Magic VLSI Layout Tool

.dc V1 0 5 0.1

efabless, ZeroAsic, Antmicro, TinyTapeout, ...



Linux Foundation Open Source Summit Europe: Open Hardware Mini Summit

NGSPICE

layout

OS to the Rescue? – IP Design

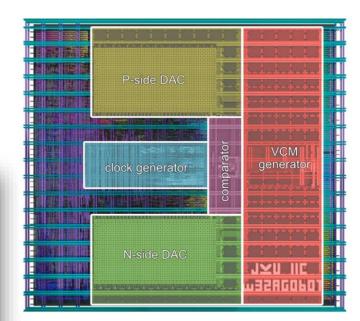


- □ Self-clocked 12-bit non-binary fully differential SAR-ADC
- □ Using SKY130 open-source PDK
- Entire mixed-signal circuit design and layout were created with free and open-source software
- Performance comparable to similar ADCs



Harald Pretl • 1st Full Professor (IC Design) @ JKU, Visiting Researcher @ IHP, fou... 6d • 🔇

Our paper (open access) describing a fully open-sourced SAR ADC IP (with fully, I mean every design file, etc., on GitHub, link in the paper) using an open-source toolchain (link in the paper) just came out. It is a nice summary and quick read; everyone who craves full detail should consult the master thesis of Manuel Moser (link in the paper).



https://link.springer.com/article/ 10.1007/s00502-023-01195-5

OS to the Rescue? - Automation



- □ Can OS help to find our holy grail "Analog Circuit Synthesis" ?
 - Today, no widely adopted solution for analog automation
 - Lots of research at different institutions, but no clear winner
 - Would need a common "condensation nucleus"
- ...better join forces?



Why OS - Enablers



People!

- OS community often fueled by individuals
- Companies step in if they see value
- Mindset change in Hardware Industry needed: See OS as opportunity, not as a threat!
- Money!
 - New Government funding requires OS: Darpa, Chips Act, Germany, ...
 - Seed funding, eg. shuttle runs

Collaborate!

- Foundations, like ChipsAlliance, OpenHWgroup
- Need common ground for "standardized" APIs



Democratizing IC Design!

- Our own first small steps...
- □ 2022 Foundation of the **MOSAIC** group
 - Modular Open Source Analog IC design framework
 - Bootcamp, <u>Gitlab</u>, <u>YouTube</u>
- 2023 Infineon Summer school
 - 50+ students invited on-site to learn about analog generators

http://www.infineon.com/schools





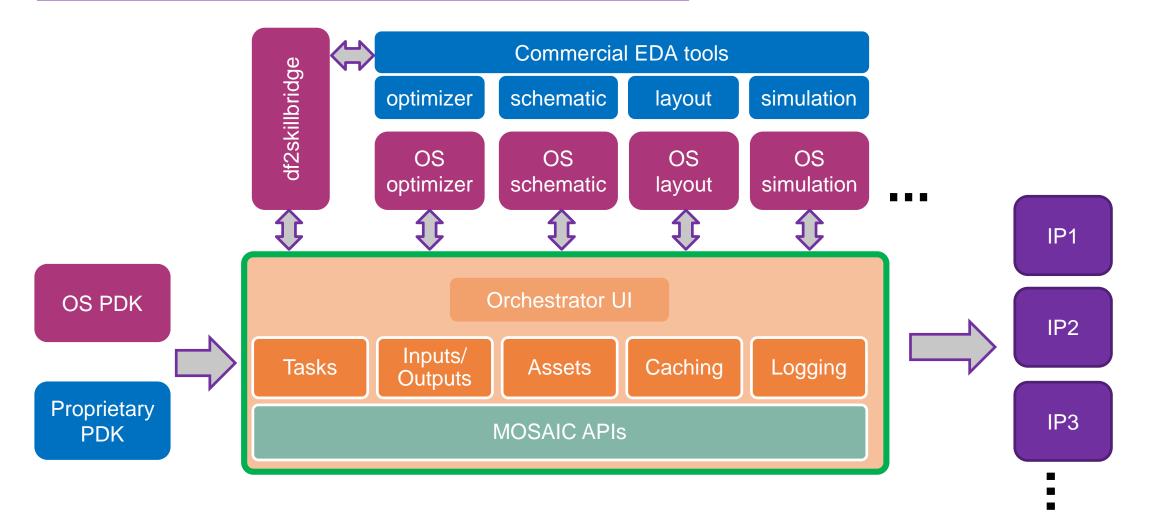
next generation of Chip Design

Linux Foundation Open Source Summit Europe: Open Hardware Mini Summit

Cinfineon

MOSAIC Analog Design Framework







- EDA toolchain: Common OS framework for analog circuit synthesis
 - ...enable various tool plugins, incl. AI applications
 - ...allowing fast creation of analog IP for different specs
 - ... create a new market for analog generator IPs
- □ SMEs to offer value-add to OS ecosystem providing new tools/plugins
- □ OS PDKs: Low entry cost to design own chip
- □ OS will ease collaborations and lower entry barrier:
 - For teaching: OS design chain is good enough already today
 - No NDA issues, easy exchange of circuit examples
 - Get funding money

How to get Industry into OS? Threats



- Business Risks:
 - Technical (eg. support)
 - Security
 - Patent
 - Giving away to competitors
 - Becoming dependent
- Organization:
 - Lack of OS experience
 - No OS approval process, no clear decision maker

Does your organization evaluate any particular business risks before allowing employees to contribute to open source projects? Check all that apply.
Technical debt
Security risk
Patent risk
Giving away technology to competitors
Becoming too dependent on technology developed by other firms
Increase likelihood of job market competition / employee turnover
None of the above

[https://www.linuxfoundation.org/research/surveys/open-source-software-funding-survey-2024]



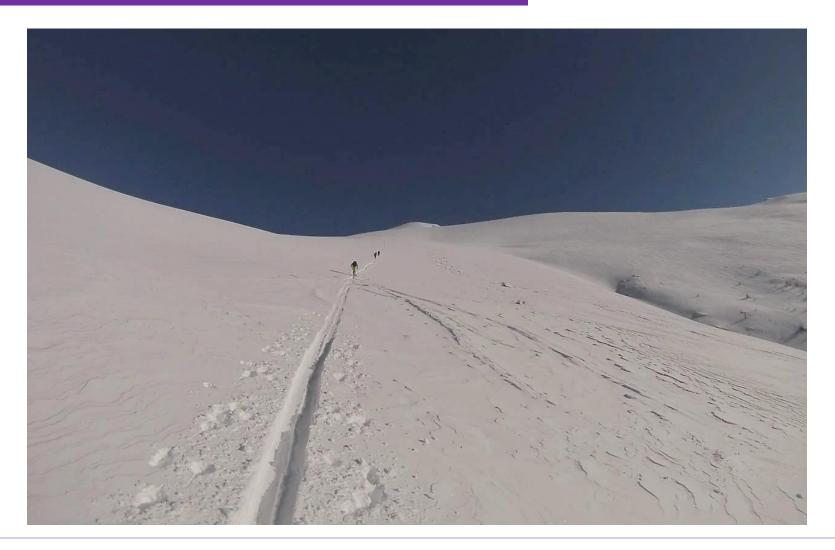
- 1. Cost efficiency: No licensing fees, share development costs
- 2. Innovation: OS projects harness creativity and expertise of a global community
- 3. Flexibility: No vendor lock-in, code can be customized
- 4. Security, Quality: Full transparency, rapid response to vulnerabilities
- 5. Talent attraction: Young engineers like OS, helps to foster new skills
- 6. Interoperability: OS and proprietary tools can be interchanged (requirement)

By leveraging these benefits, industries can drive innovation, reduce costs, and maintain a competitive edge in a rapidly evolving technological landscape.

[partly GPT4.0]

2024: We continue, step by step...





References



...this is just an incomplete list of some interesting links to probe further:

- https://sscs.ieee.org/about/solid-state-circuits-directions/sscs-pico-program
- https://open-source-eda-birds-of-a-feather.github.io/ (OS EDA session at DAC 2023)
- https://tinytapeout.com/
- https://gitlab.com/mosaic_group/mosaic_BAG/virtuoso_template
- https://www.youtube.com/@mosaic6083
- □ <u>https://www.chipsalliance.org/</u>
- https://www.openhwgroup.org/
- https://chipyard.readthedocs.io/en/stable/index.html
- https://developers.google.com/silicon
- https://bit.ly/esscxxrc22-goog
- □ <u>https://www.klayout.de/</u>
- https://laygo2.github.io/
- https://github.com/idea-fasoc/OpenFASOC
- http://opencircuitdesign.com/magic/
- https://github.com/ALIGN-analoglayout/ALIGN-public
- https://github.com/The-OpenROAD-Project/OpenLane
- https://bag3-readthedocs.readthedocs.io/en/latest/
- □ <u>https://niftylab.github.io/</u>
- https://github.com/iic-jku/osic-multitool
- □ <u>https://link.springer.com/article/10.1007/s00502-023-01195-5</u>
- □ <u>http://www.infineon.com/schools</u>



This work is funded by the Austrian Federal Ministry of Climate Action, Environment, Energy, Mobility, Innovation and Technology, the Austrian Federal Ministry of Digital and Economic Affairs, and implemented by austria wirtschaftsservice (aws) and the Austrian Research Promotion Agency (FFG)

in the frame of the

Important Project of Common European Interest (IPCEI) on Microelectronics and Communication Technologies (ME/CT).

Federal Ministry Republic of Austria Climate Action, Environment, Energy, Mobility, Innovation and Technology Federal Ministry Republic of Austria Digital and Economic Affairs





